EG915U Series

Reference Design

LTE Standard Module Series

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Status: Released

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About the Document

Revision History

Version	Date	Author	Description
-	2021-09-18	Reuben WANG/ Ailsa WANG/ Frank WANG	Creation of the document
1.0	2021-10-26	Reuben WANG/ Ailsa WANG/ Frank WANG	First official release

Contents

1 Reference Design

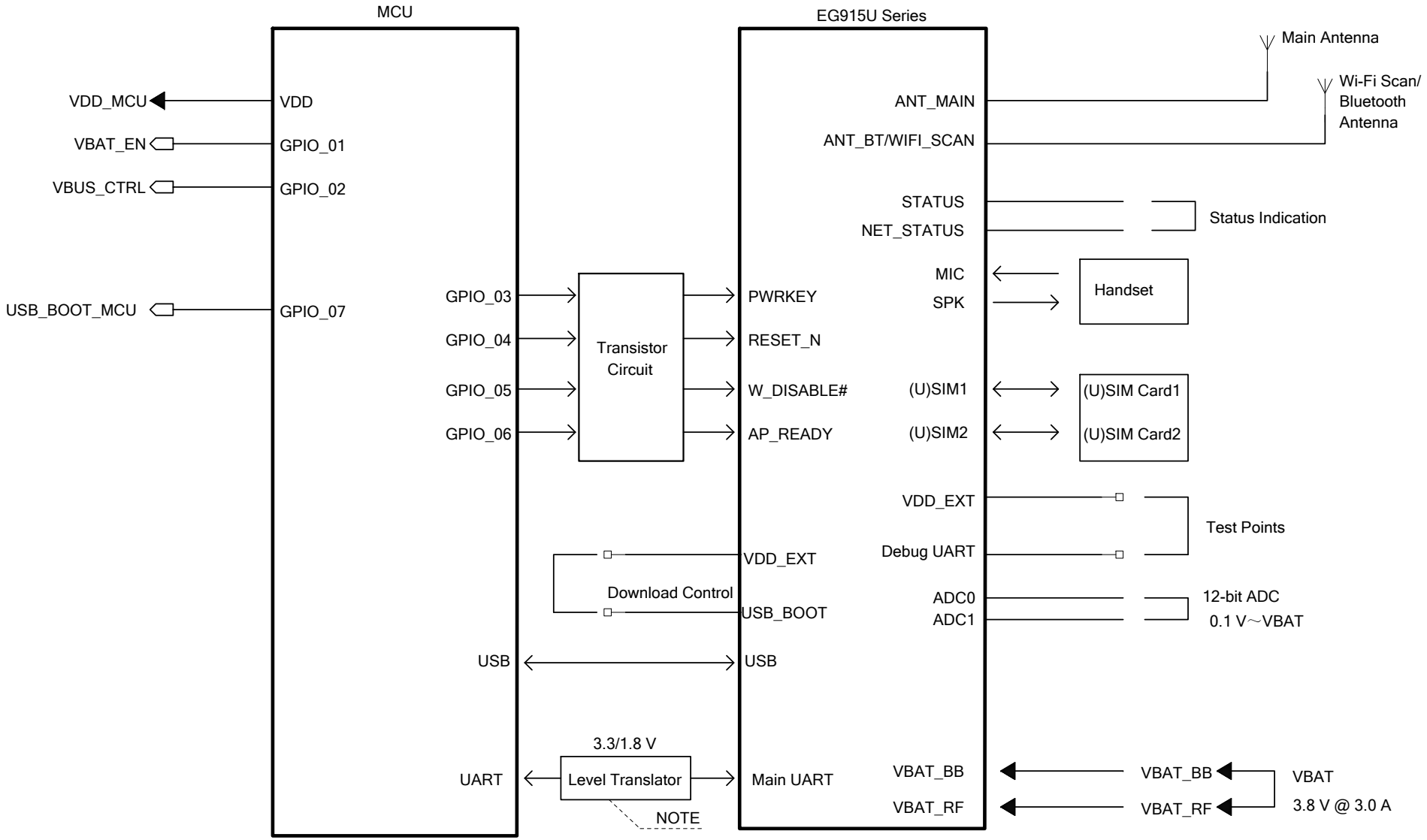
1.1. Introduction

This document provides the reference design for Quectel EG915U series module, including the design of power supply, UART, (U)SIM, audio interfaces, etc.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Reference Design Block Diagram



NOTE:

A level-shifting circuit with triode or a level translator TXS0108EPWR provided by Texas Instruments is recommended.

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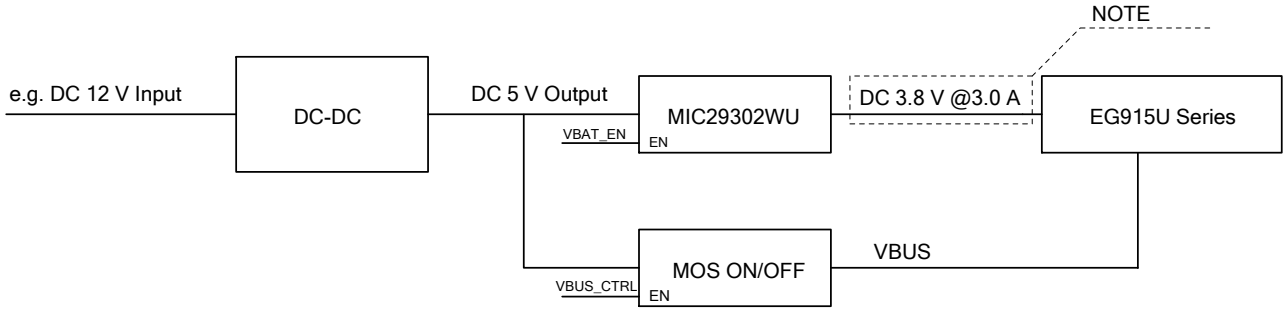
Power Supply Block Diagram



NOTE:

For EG915U series, the power supply should be 3 A current at least.

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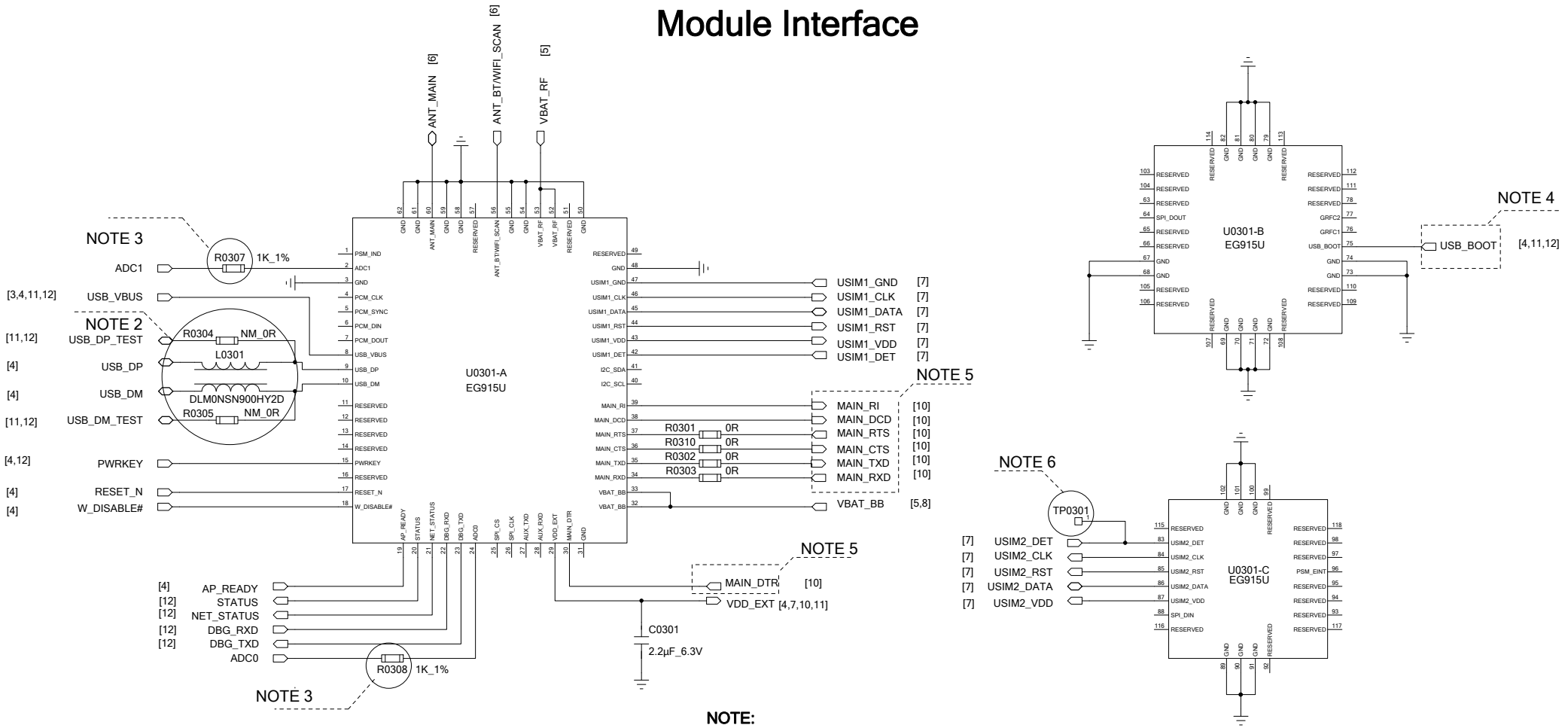
Module Interface



NOTE:

1. Unused and RESERVED pins are kept open, and all GND pins are connected to the ground network.
2. A common mode choke L0301 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission, and it should be placed close to the module.
   Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra stubs of the trace. The two resistors should be placed close to the module to ensure the integrity of USB signal.
3. When using the ADC pin, a 1 kΩ resistor must be connected in series.
   If there is a need of divider resistors, the resistance needs to be no more than 100 kΩ. Otherwise, the measurement accuracy of the ADC will be significantly reduced.
4. USB_BOOT cannot be pulled up before startup.
5. For more information about the main UART interface, please refer to *Quectel_EG915U_Series_Hardware_Design*.
6. Reserve the test point to capture cp logs.

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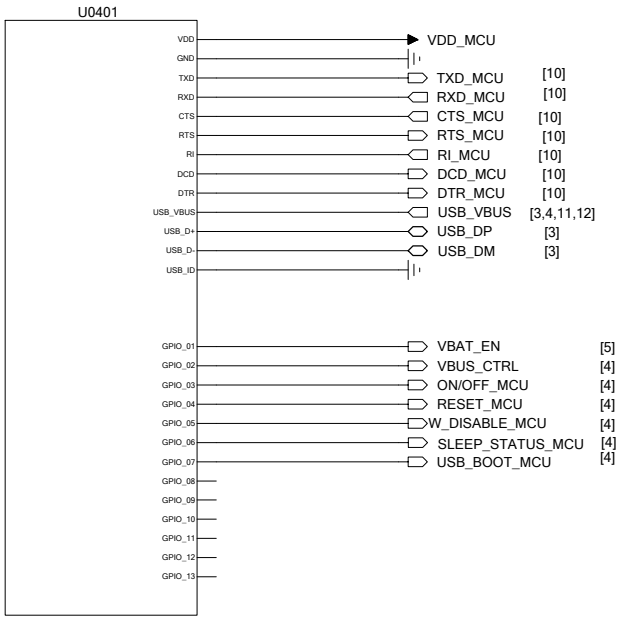
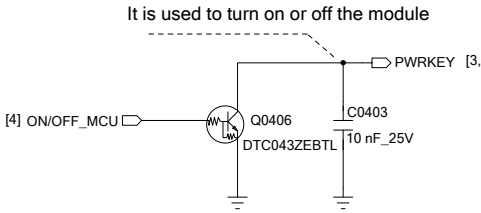
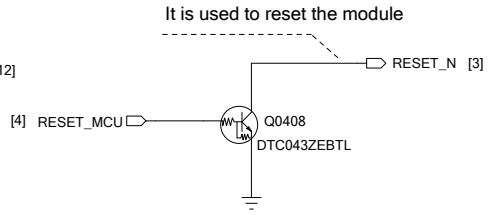
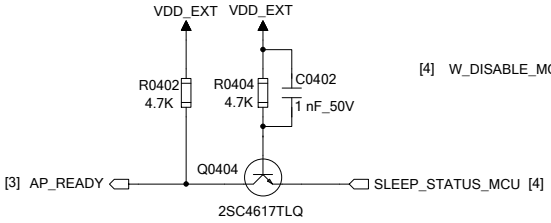
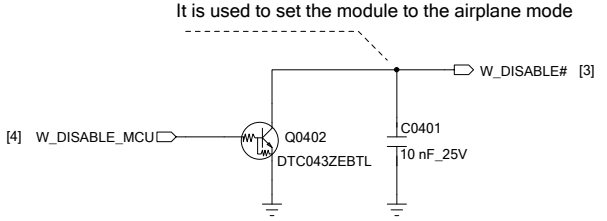
MCU Interface

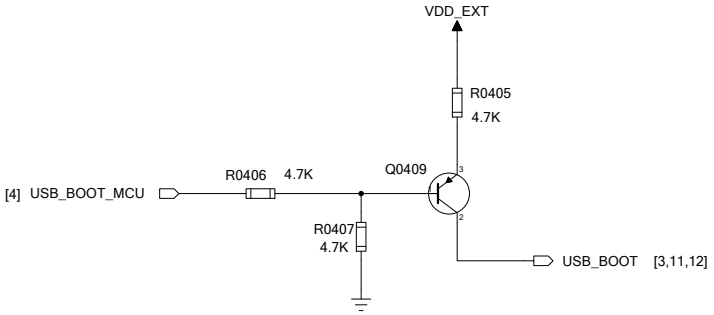


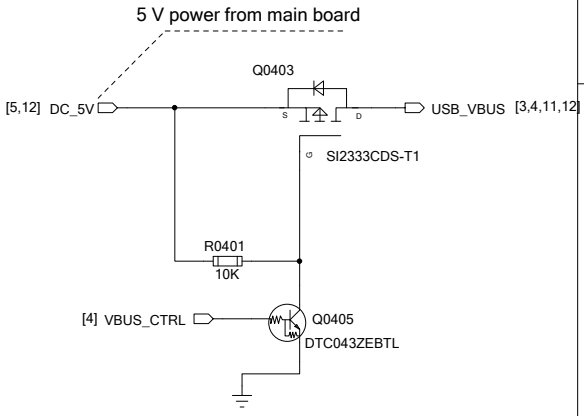












NOTE:

1. U0401 represents customer's MCU. The power domain of GPIO interfaces of EG915U series module is 1.8 V;
   if the GPIO interfaces of U0401 share the same power domain, then the related level-shifting circuit is not needed.
2. The USB interface of EG915U series can only serves as a slave device and supports high-speed and full-speed modes of USB 2.0.
   To communicate with the USB interface, MCU needs to support USB host mode or OTG function. The USB_VBUS pin of the module and MCU should be powered by an external power system, and the pin of the module is for USB detection. VBUS_CTRL is used to turn on/off the USB_VBUS power supply.
3. It is recommended to select the default low-level GPIOs of MCU as the control pins for PWRKEY and RESET_N of the module.
   Please ensure that the maximum load capacitance of pin PWRKEY and RESET_N does not exceed 10 nF.
4. To prevent the module from staying in download mode due to the turn-on of triode Q0209 after the MCU's power-on, the USB_BOOT_MCU pin needs to be at high level by default when the MCU is powered on.
   For the same purpose, if the triode control method is not used, the method of reserved pins or key press can be used.

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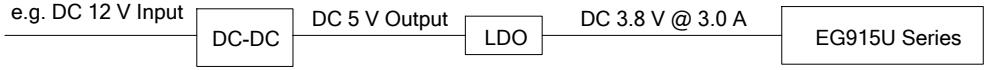
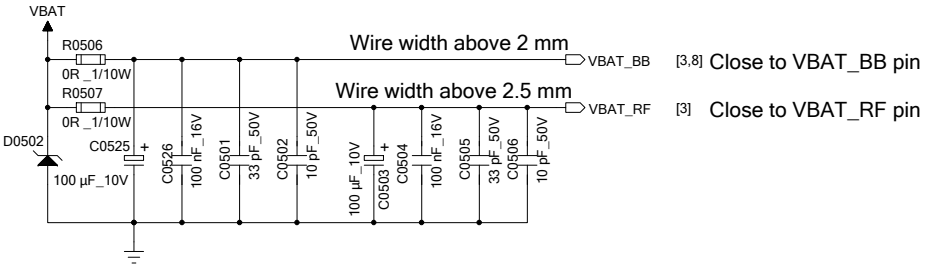
Power Supply Design

DC-DC Application

When the input voltage exceeds 7.0 V, use a DC-DC to convert it to an output voltage of 5.0 V, and then convert it to 3.8 V through an LDO to supply power to the module.



VBAT Design

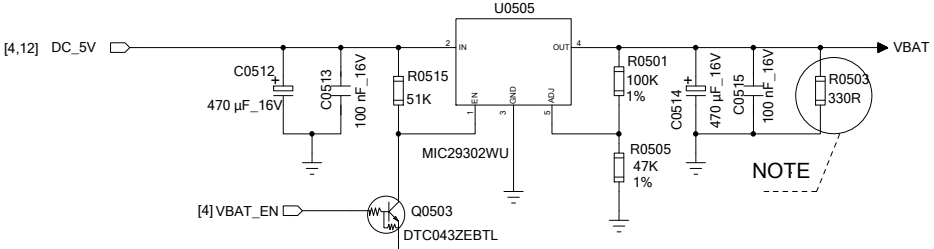


NOTE:

1. For EG915U series, the power supply should be 3 A current at least.
2. VBAT should be routed in star structure to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3-4.3 V,typ 3.8 V.

LDO Application

It is used when the input voltage is below 7.0 V. Use an LDO IC to convert the input voltage to 3.8 V.



VBAT = (R0501/R0505 + 1) × 1.24 = 3.88 V

NOTE: The recommended load current is not less than 10 mA.

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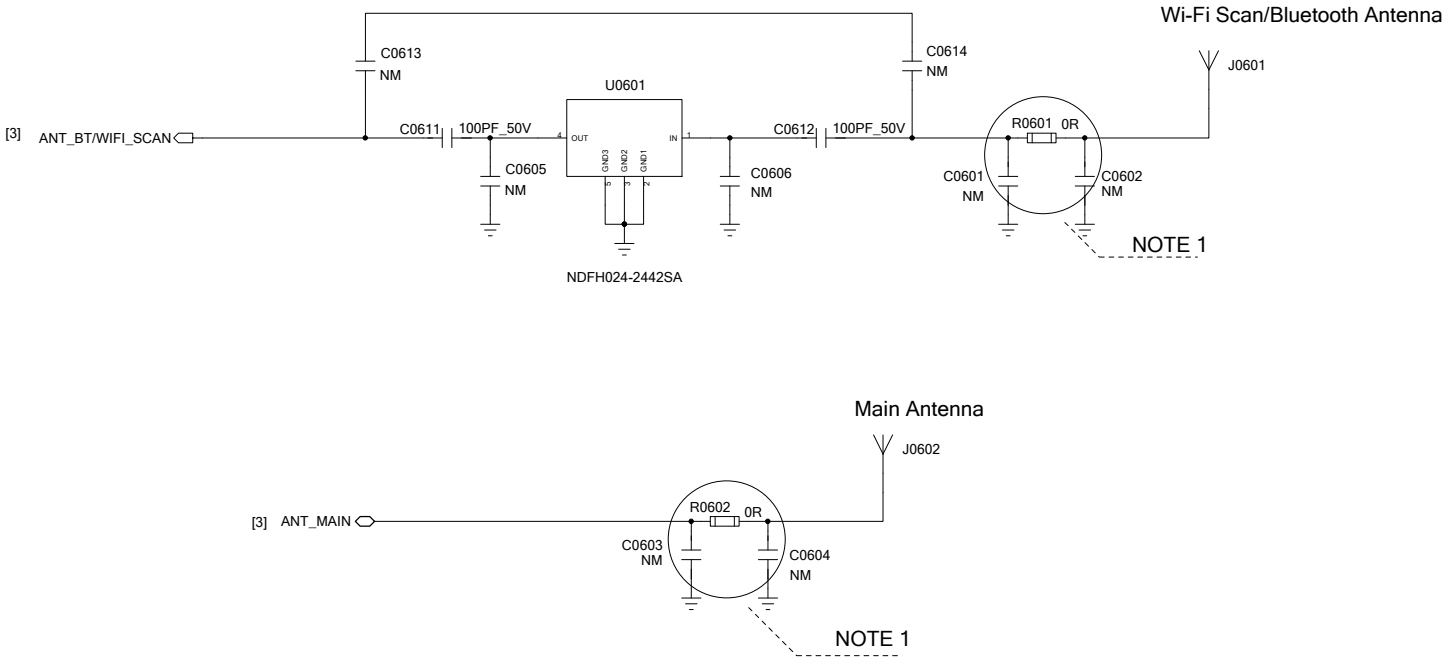
Antenna Interface Design



NOTE:

1. It is highly recommended to reserve a Π type main antenna circuit for future debugging.
2. The single-ended impedance of the RF antenna is 50 Ω.
3. For EG915U-CN, you can select C0613 & C0614 in the compatible design, and C0605 & C0606 & C0611 & C0612 & U0601 are not mounted by default.
4. For EG915U-EU/-LA, you can select C0605 & C0606 & C0611 & C0612 & U0601 in the compatible design, and C0613 & C0614 are not mounted by default.

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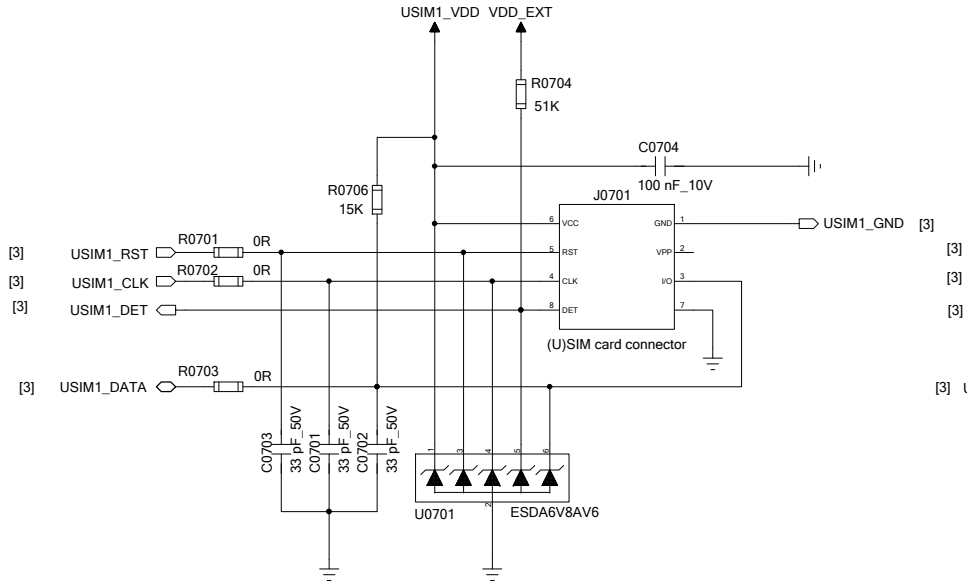
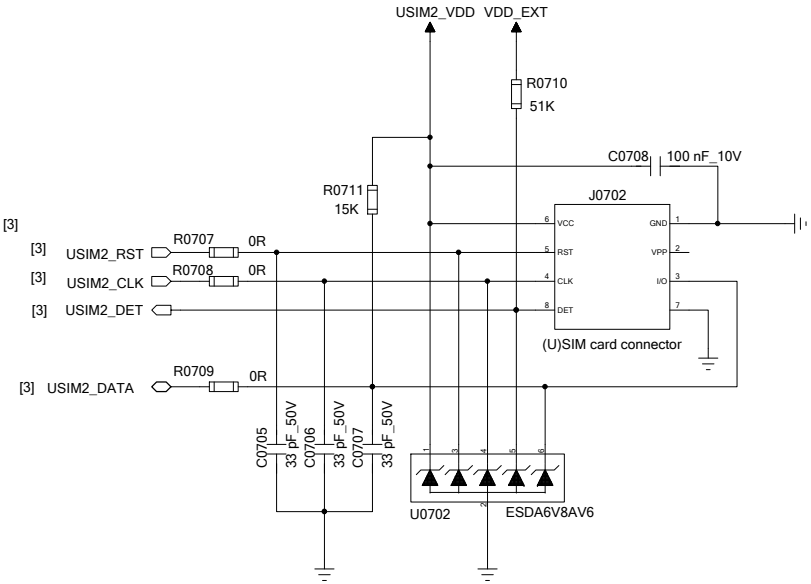
(U)SIM Interface Design

(U)SIM1



(U)SIM2



NOTE:

1. U0701 & U0702 are recommended to be used to offer good ESD protection, and the parasitic capacitance should not be more than 15 pF.
2. The pull-up resistors R0706 & R0711 can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.
3. R0701-R0703 & R0707-R0709 are used for debugging, and C0701-C0703 & C0705-C0707 are used for filtering out RF interference.
4. C0704 & C0708's capacitance should be less than 1 μF and they should be placed close to the (U)SIM card connector.
5. The GND of the (U)SIM card connector is recommended to be connected to the main GND layer directly.
6. (U)SIM_DET is disabled by default, you can configure high level or low level detection as hot-plug detection.
7. For more information about the layout of (U)SIM interface, please refer to *Quectel_EG915U_Series_Hardware_Design.*

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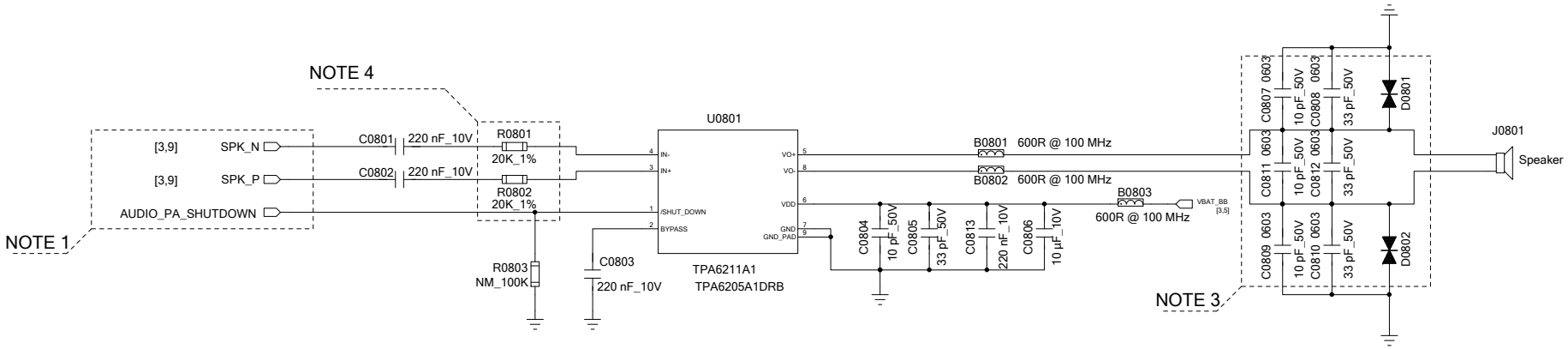
Analog Audio Design (Loudspeaker)



NOTE:

1. SPK_N and SPK_P are differential outputs. In order to eliminate POP sound, it is recommended to choose one of the GPIO pins of the module as the AUDIO_PA_SHUTDOWN pin for signal enablement of the power amplifier. For details, please contact Quectel Technical Supports.
2. Choose the audio power amplifier with appropriate power according to the actual needs .
3. Place filter capacitors and ESD protection components close to the loudspeaker.
4. Audio PA Gain = 40 kΩ / R0801 or R0802.

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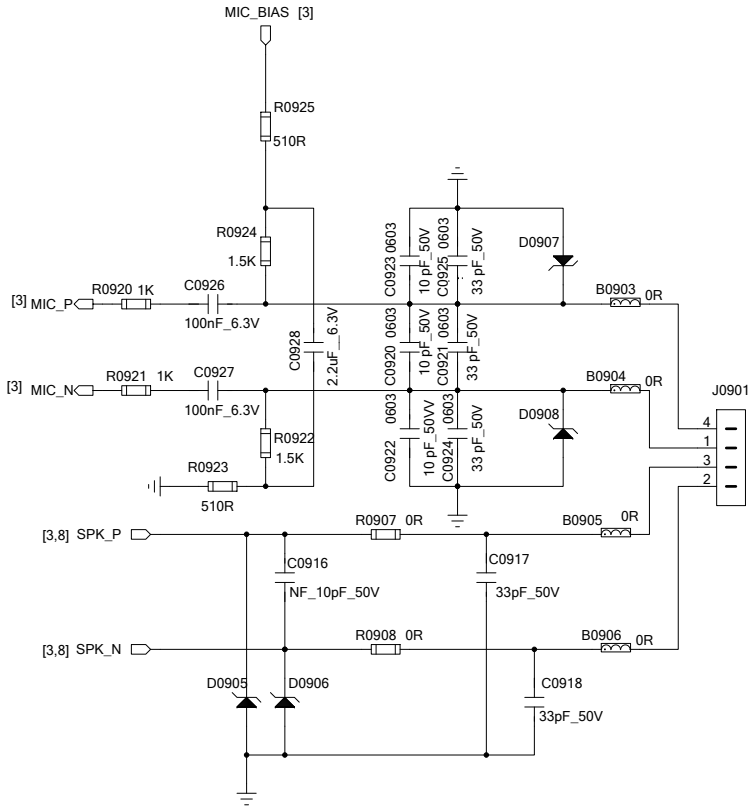
Analog Audio Design (Headset)



NOTE:

1. Both the MIC and SPK signal traces need to be routed as differential pairs.
2. All MIC and SPK signal traces should be surrounded with ground on the layer and with ground planes above and below, and far away from noises sources.

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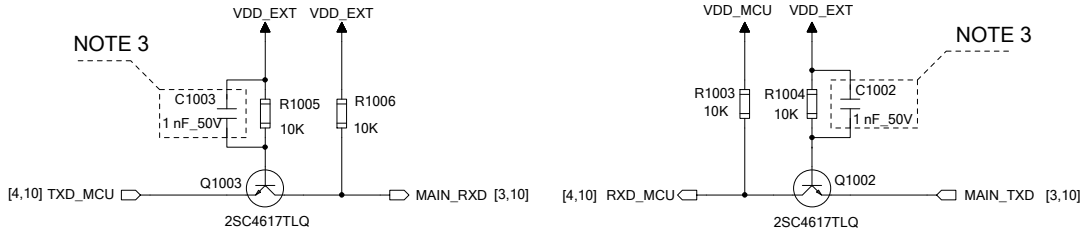
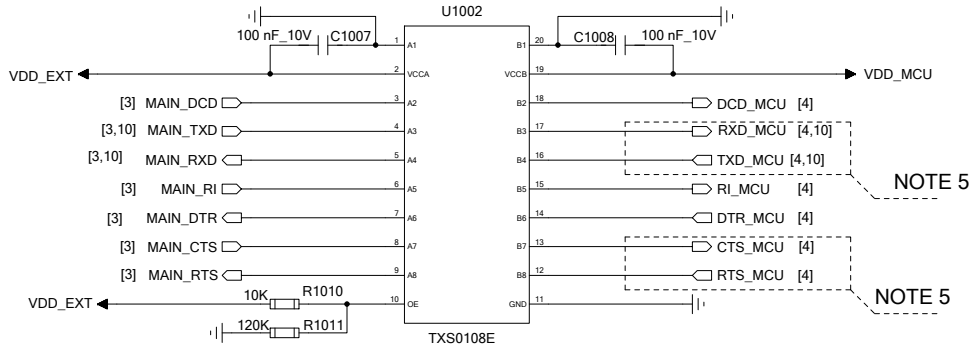
UART Interfaces Design

UART Level Conversion - Triode Solution



UART Level Conversion - IC Solution



NOTE:

1. There are two translation solutions: transistor solution and IC solution, of which the latter is recommended.
2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet of TXS0108EPWR.
3. The transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps. The capacitors C1002 and C1003 of 1 nF can improve the signal quality.
4. The MAIN_RTS and MAIN_DTR troide transistor circuits are similar to that of the MAIN_RXD.
   The MAIN_CTS, MAIN_RI and MAIN_DCD troide transistor circuits are similar to that of the MAIN_TXD.
5. The hardware flow control pins CTS and RTS adopt the direct connection mode, that is, the RTS of the module is connected to the RTS of the MCU, and the CTS of the module is connected to the CTS of the MCU. Pay attention to the direction of signal input and output.
   TXD and RXD adopt a cross connection mode, that is, the TXD and RXD of the module are respectively connected to the RXD and TXD of the MCU.

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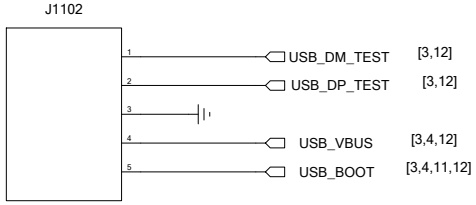
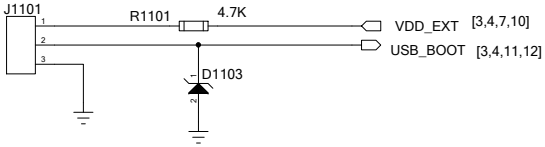
Download Method

USB Download Interface Design



USB_BOOT Interface Design Method



NOTE:

1. When the module needs to upgrade the firmware, it shall first enter the download mode by connecting the USB_BOOT and VDD_EXT before power-on, and the module will enter download mode after power-on ;
2. Be sure to reserve the USB_BOOT interface circuit to upgrade the firmware.

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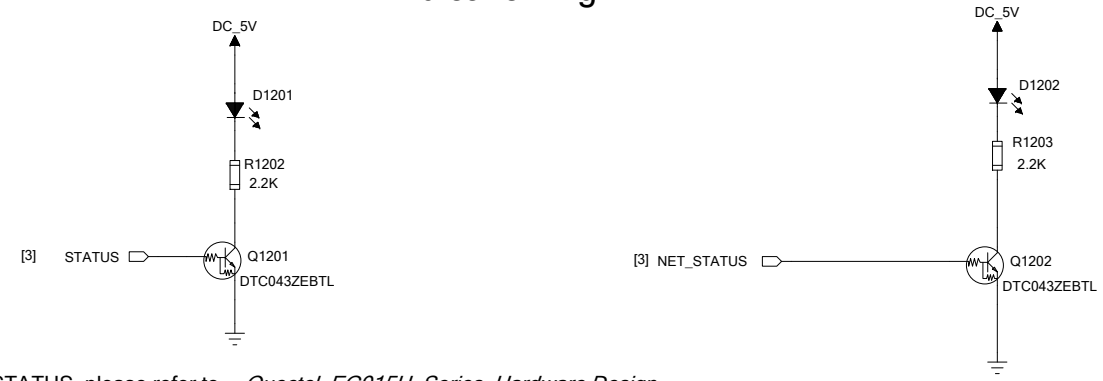
Other Designs

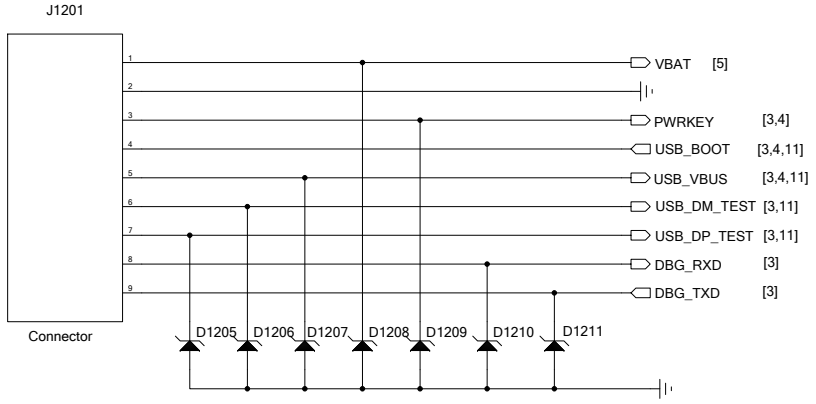
Indication Light



NOTE:

1. For more details about STATUS and NET_STATUS, please refer to *Quectel_EG915U_Series_Hardware Design*.
2. If the low power consumption is required when the customers' device is in sleep status, replace the power supply DC_5V of the lights with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.

Reserved Test Points



NOTE:

1. Test points for both USB and debug UART interfaces are recommended to be reserved for capturing logs; the USB interface can also be used to upgrade the firmware of the module.
2. The parasitic capacitance of the ESD protection componets on USB data traces should be less than 2 pF.
3. Debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of customers' application is 3.3 V. For details, please refer to "UART Interfaces Design". The debug serial port only supports the baud rate of 921600 bps.
4. When the module needs to upgrade the firmware, it must first enter the download mode. Please refer to "Download Method" for the download circuit design.

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